American Standard Circuits

Sunstone Circuits

ULTRA-HDI & ADVANCED PACKAGING

Using Semi-Additive Process — ASC now provides our customers with 12.5µ trace and space fabrication!

As a pioneer in North America's electronics sector, we were early in adopting the groundbreaking ultra high-density interconnect technology, A-SAP™, from Averatek Corporation. Going as far as supplementing the process with ultra thin foils to augment our SAP technology. Securing our role, as the leader of the vanguard in ultra-fine lines and spaces for rigid, rigid-flex, and flex PCBs.

Explore how making ***tiny*** spaces & traces using Ultra-HDI can make a ***HUGE*** impact on your PCBs.

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THE ADVANTAGES

RELIABILITY
Ultra high-density fabrication reduces layer count, micro-vias, and lamination cycles, ultimately improving reliability.

SIGNAL INTEGRITY
Improved quality with aspect ratios greater than 1:1 for metal traces.

HIGH PERFORMANCE PCB
Improved RF performance over traditional subtractive-etch processes.

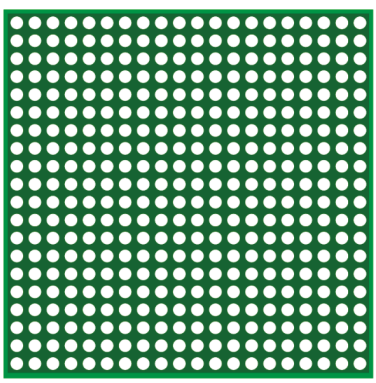
PACKAGE SUBSTRATES & INTERPOSERS
Dramatic size and weight reduction over current state-of-the-art productions with 12.5µ (0.5mIl) trace and space.

DESIGN
Tight spacing and impedance control (< 5%) for all line widths.

GOLD!
Biocompatibility for utilization of gold as conductive metal.

STANDARD PCB

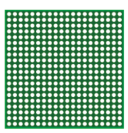
19mm (enlarged)



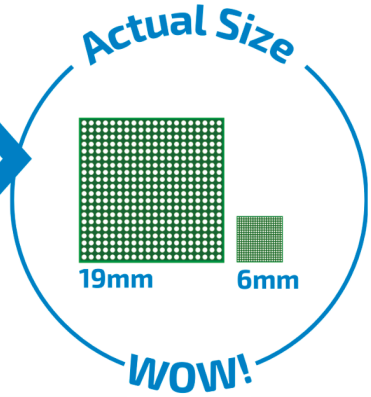
0.8mm pitch - 20x20 grid
3 routing layers - L/S 3mil/3mil

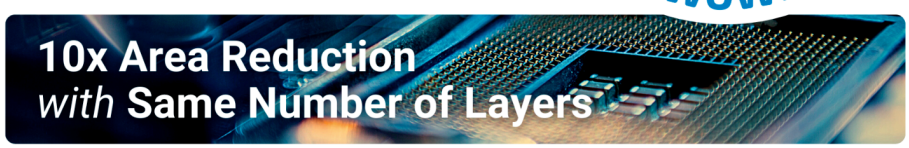
UHDI PCB

6mm (enlarged)



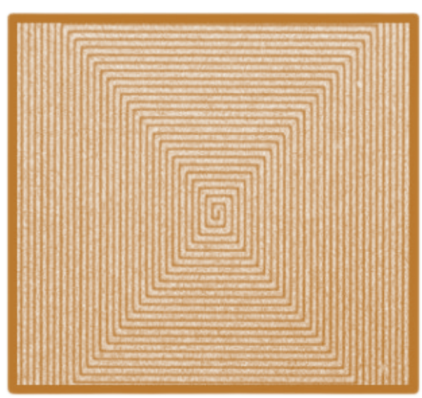
0.3mm pitch - 20x20 grid
3 routing layers - L/S **1mil/1mil**





75µ
Standard
1x density

25µ
mSAP
9x density



12.5µ
Ultra-HDI
36x density

A LITTLE "NO"

DO ALL LAYERS OF A BOARD NEED TO BE PRODUCED WITH THESE ULTRA-HIGH DENSITY FEATURE SIZES?

No—both subtractive-etch layers and UHDI layers can be used in the same PCB stack-up. All layers do not have to be the same technology: a hybrid approach is most common.

Typically, signal layers will utilize UHDI technology to simplify the breakout of smaller BGA packages, reducing the number of layers and lamination cycles required. For layers that contain only larger feature sizes, traditional subtractive-etch technology can be used.

WHAT IS THE MAXIMUM NUMBER OF LAYERS AND NUMBER OF LAMINATION CYCLES FOR UHDI TECHNOLOGY?

No Limits—With the smaller features, it makes sense to focus on designs that can increase reliability by minimizing stacked vias. This avoids additional costs resulting from processing stacked structures.

Similarly, the use of ultra-fine lines should also focus on the elimination of micro-via structures, especially multiple stacks of micro-vias, to minimize reliability issues and additional costs resulting from processing the stacked structures.

A LOT OF "YES"

CAN UHDI SAVE ME MONEY?

Yes—utilizing Ultra-HDI can reduce layer count, lamination cycles, and overall design complexity. While UHDI can cost more than subtractive etch, this simplification of your design may reduce total costs or provide added functionality in a similar cost structure.

ARE PCBS MADE WITH UHDI AS RELIABLE AS THOSE TRADITIONALLY FABRICATED?

Yes—UHDI is a proven and tested additive fabrication method to achieve next-generation advancements.

CAN OUTER LAYERS AND PLATED THROUGH HOLES BE CREATED WITH UHDI?

Yes—You can confidently design a PCB with Ultra-HDI features on outer layers and connect with reliable plated through holes, using the UHDI process.

CAN UHDI PROCESSES ALSO PRODUCE LARGER FEATURE SIZES?

Yes—UHDI is not just for Ultra-HDI. There are signal integrity benefits to semi- additive processes that make it preferable for larger feature sizes as well.

IS UHDI CAPABLE OF COPPER VIA FILL, NON-CONDUCTIVE VIA FILL, AND VIA-IN-PAD-PLATED-OVER (VIPPO)?

Yes, Yes, and Yes!—for non-conductive via fill, the vias must be >150µ.

Via-in-pad structures should be run on non UHDI layers. If needed, these structures should be used in an external mixed power/ground structure with limited traces and line widths of 3 mils with 5 mil spacing.

If via-in-pad is necessary along with ultra- fine lines: a copper-filled micro-via should be used to route to the next layer down. This via should be 3 to 4 mils diameter, and the dielectric spacing should be no greater than the via diameter, preferably less - aspect ratio 1:1 max.

If top and bottom layers of the subassembly do not require ultra-fine line width technology: a buried via structure may be used. This via may be filled and plated over.

HELPFUL ULTRA-HDI WHITEPAPERS

Design 1 | Design 2 | BGAs

TIPS & CONSIDERATIONS

SOLDERMASK

For ultra-fine line external layers should define pads as 'mask defined' instead of 'metal defined' pads.

This will prevent registration issues exposing the adjacent metal when the external spacing is less than 50µ (2 mils) between the pad and adjacent metal.

REFLECTIONS

In a uniform 50 ohm trace, reflections affect signal quality in narrow regions i.e. shorter traces mitigate reflections.

MINIMUM SPACING

If pads are defined by the mask—spacing can be as low as 25µ.

If defined by the copper—other features need to be at least 50µ if not 75µ away.

The copper to copper spacing can add costs in subtractive etch processes—with UHDI, this is not the case!

On inner layers, spacing can be ≤25µ. On outer layers, there must be enough space to allow the soldermask to fully cover the trace and not expose any copper. If the mask defines the pad, the coverage is not an issue so 25µ can work. If not, mask registration allowances need at least 50µ spacing or more.

Parameter	Minimum Microns (µ)	Notes
Line width	15 (±5%)	Tolerance applies to trace widths up to 50µ (±2.5µ for wider lines)
Line space	12.5 (±5%)	
Line copper thickness >50µ lines	10–40 (±5%)	
Line copper thickness of 25µ lines	35 max (±5%)	
Line copper thickness of 12.5—20µ lines	20 max (±5%)	
Microvia hole diameter	75	Rigid—50µ thick material or less
Microvia pad diameter	200	Advanced—50µ via in 25µ flex
Through hole diameter	150	100µ for 0.8mm thick boards
Through hole pad diameter	300	200µ for 100µ hole diameter in 0.8mm thick boards
Via Clearance to Board Edge (Laser Cut)	125	Edge of pad or trace to board edge
Via Clearance to Board Edge (Mech Route)	250+	
Copper thickness in thru holes	25 nominal	
Copper thickness in microvia	25 nominal or copper-filled	

FOR MORE INFORMATION

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