TAKING OUR CUSTOMERS TO THE NEXT LEVEL

AMERICAN STANDARD CIRCUITS

ULTRA HDI & ADVANCED PACKAGING OFFERING

THE ADVANTAGES

WIth the A-SAP™ manufacturing process, ASC now provides our customers with 20-micron trace/space

Ultra high-density

Improves reliability

reduce layer count, micro vias and lamination cycles

Improved Signal Integrity

aspect ratios greater than 1:1 for metal traces

High Performance PCB

Improved RF Performance

over traditional subtractive-etch processes

Biocompatibility:

capability for utilization of gold as conductive metal

Package Substrates & Interposers

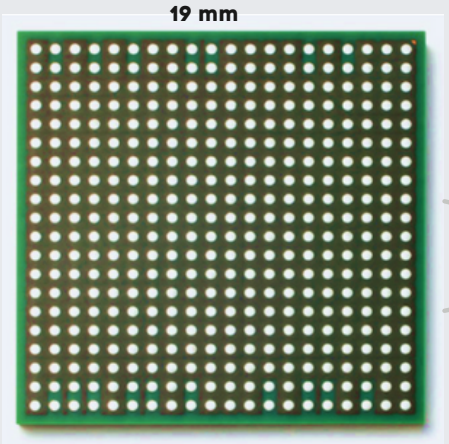
Dramatic size and weight reduction

over current state-of-the-art with 12.5-micron (.5mIl) trace and space

Design

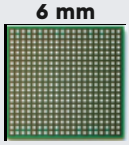
Tight spacing and impedance

control (< 5%) for all line widths



Standard PCB

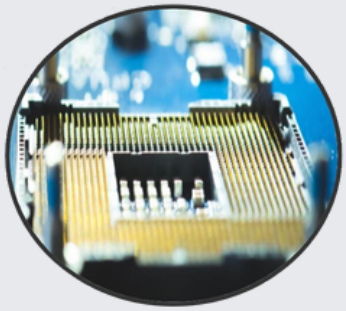
0.8 mm pitch - 20x20 grid
3 routing layers - L/S 3 mil/3 mil



A-SAP PCB

0.3mm pitch - 20x20 grid
3 routing layers - L/S **1 mil/1 mil**

10X Area Reduction
with Same Number Of Layers



FAQs

DO ALL LAYERS OF A BOARD NEED TO BE PRODUCED WITH THESE ULTRA-HIGH DENSITY FEATURE SIZES?

NO.

Both subtractive-etch layers and A-SAP™ layers can be used in the same PCB stack-up. All layers do not have to be the same technology: a hybrid approach is most common.

Typically, signal layers will utilize A-SAP™ technology to simplify the breakout of smaller BGA packages, reducing the number of layers and lamination cycles required. For layers that contain only larger feature sizes, traditional subtractive-etch technology can be used.

WHAT IS THE MAXIMUM NUMBER OF LAYERS AND NUMBER OF LAMINATION CYCLES FOR A-SAP™ TECHNOLOGY?

THERE IS NO LIMIT.

With the smaller features, it makes sense to focus on designs that can increase reliability by minimizing stacked vias. This avoids additional cost resulting from processing the stacked structure.

Ideally, the use of ultra-fine lines should also focus on the elimination of microvia structures, especially multiple stacked microvias, to minimize reliability issues from stacked microvias and the additional cost resulting from processing the stacked structures.

CAN A-SAP™ PROCESSES ALSO PRODUCE LARGER FEATURE SIZES?

YES. A-SAP™ IS NOT JUST FOR ULTRA HDI.

There are signal integrity benefits to semi-additive processes that make it preferable for larger feature sizes as well.

CAN OUTER LAYERS AND PLATED THROUGH HOLES BE CREATED WITH A-SAP™?

YES.

You can confidently design a PCB with ultra hdi features on outer layers and connect with reliable plated through holes, using the A-SAP™ process.

WHAT IS THE MINIMUM SPACING FROM TRACE TO PAD (EXTERNAL LAYER)?

THAT DEPENDS ON HOW PADS ARE DEFINED BY SOLDERMASK- IF PADS ARE MASK DEFINED, SPACING CAN BE AS LOW AS 25 MICRON. IF DEFINED BY THE COPPER, THEN OTHER FEATURES NEED TO BE AT LEAST 50 MICRONS AWAY, PREFERABLY 75 MICRONS.

The copper to copper spacing can add costs in subtractive etch processes. In the semi-additive environment, this is not the case.

1. On inner layers, spacing could be 25 microns or below.
2. For outer layers, there must be enough space to allow the soldermask to fully cover the trace and not expose any copper. If the mask defines the pad, the coverage is not an issue so 25 micron can work. If not, mask registration allowances need at least 50 micron spacing or more.

FAQs

RELIABILITY: ARE PCBS MADE WITH A-SAP™ AS RELIABLE AS THOSE FABRICATED WITH TRADITIONAL PROCESSES?

YES.

The Averatek Semi-Additive Process (A-SAP™) is a proven and tested additive fabrication method to achieve next-generation advancements. Contact us for more information.

WHAT ARE DESIGN CONSIDERATIONS WHEN DESIGNING WITH VIA-IN-PAD-PLATED-OVER (VIPPO)?

Via-in-pad structures should be run on non-A-SAP™ layers. If needed, these structures should be used in an external mixed power/ground structure with limited traces and line widths of 3 mils with 5 mil spacing.

If via-in-pad is necessary along with ultra-fine lines: a copper-filled microvia should be used to route to the next layer down. This via should be 3 to 4 mils diameter, and the dielectric spacing should be no greater than the via diameter, preferably less - aspect ratio 1:1 max.

If top and bottom layers of the subassembly do not require ultra-fine line width technology: a buried via structure may be used. This via may be filled and plated over.

COST: HOW DOES A-SAP™ COMPARE TO SUBTRACTIVE ETCH?

A-SAP™ HAS POTENTIAL TO LOWER COSTS.

One primary benefit of ultra HDI is the ability to reduce layer count, reduce lamination cycles and reduce the complexity of the PCB design. While A-SAP™ processing costs can be higher than subtractive etch, the overall simplification of the design may reduce total costs or provide added functionality within a similar cost structure.

WHAT IS TYPICAL STACK UP FOR A 50 OHM IMPEDANCE REQUIREMENT?

One primary benefit of ultra HDI is the ability to reduce layer count, reduce lamination cycles and reduce the complexity of the PCB design. While A-SAP™ processing costs can be higher than subtractive etch, the overall simplification of the design may reduce total costs or provide added functionality within a similar cost structure.

TRACE IMPEDANCE: WHAT DOES ASC RECOMMEND WHEN DESIGNING WITH IMPEDANCE CONTROL REQUIREMENTS AND ULTRA HDI FEATURE SIZES?

There have been three white papers published to help PCB designers understand how to best address this and our team is happy to help answer any questions.

TO CONSIDER...

Soldermask for ultra-fine line external layers should define pads as ‘mask defined’ vs ‘metal defined’ pads. This will prevent soldermask registration issues exposing the adjacent metal when the external spacing is less than 50 microns (2 mils) between the pad and adjacent metal.

ULTRA HDI CAPABILITIES

Parameter	Minimum (Micron)	Comments
Line width	15 (+/-5%)	Tolerance applies to trace widths up to 50 microns +/-2.5 microns for wider lines
Line space	12.5 (+/-5%)	
Line copper thickness (> 50 micron lines)	10-40 (+/-5%)	
Line copper thickness (25 micron lines)	25 max (+/-5%)	
Line copper thickness (12.5-20 micron lines)	20 max (+/-5%)	
Microvia hole diameter	75	Rigid: 50 um thick material or less
Microvia pad diameter	200	Advanced: 50 um via in 25 um flex
Through hole diameter	150	100 micron for 0.8 mm thick boards
Through hole pad diameter	300	200 micron for 100 micron hole dia. for 0.8 mm thick boards
Via Clearance to Board Edge (Laser Cut)	125	Edge of pad or trace to board edge
Via Clearance to Board Edge (Mech route)	250+	
Copper thickness in thru holes	25 nominal	
Copper thickness in microvia	25 nominal	
Copper Via Fill	Yes	
Non-Conductive Via Fill	Yes	Vias larger than 150 microns
Via-In-Pad-Plated-Over (VIPPO)	Yes	See recommendation in FAQs

A Summary of Our **Company Profile**

ASC is a total solutions provider for quality PCB manufacturing: rigid, flex, rigid-flex, RF/microwave, and metal-backed. With the expertise to provide a variety of technologies in a time-critical environment, our capabilities range from test and prototypes to high-volume production. Qualifications include:AS9100 Rev D, ISO 9001:2015, ISO13485:2016, IATF16949:2016, MIL-PRF-31032, MIL-PRF-55110, MIL-PRF-50884 certification.

Learn more about our cutting-edge solutions at technology@asc-i.com

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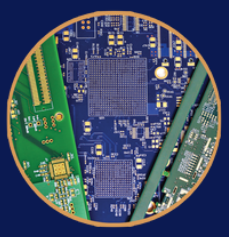
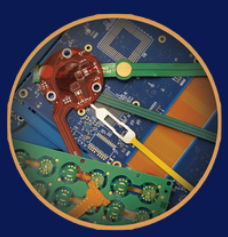
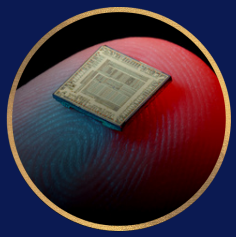
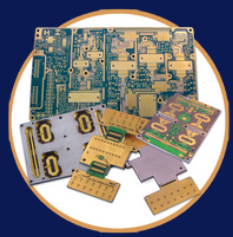
PRODUCTS

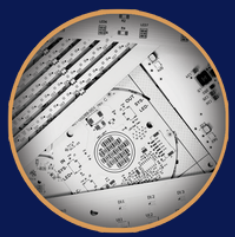

Digital PCB's


RF/Microwave


Flex Rigid-Flex


Ultra HDI


RF Metal Backed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